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Design and Implementation of a Power-Efficient HML-BIST Architecture for BCD Multiplier Testing

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Abstract: *Built-in self-test (BIST) reduces dependence on external test equipment by generating test patterns and evaluating responses on-chip. However, conventional pseudo-random BIST can produce excessive switching activity during test, increasing test power and potentially creating misleading failures in deeply integrated VLSI systems. This paper presents an HML-BIST architecture for a BCD multiplier test environment that combines linear-feedback shift-register (LFSR) based pattern generation, explicit activity-factor control, RAM-based storage, and a space comparator for response verification and fault indication. Separate LFSR paths are used to exercise write data, write address, and read address operations, while the activity-control mechanism regulates pattern transitions. Stuck-at-0 and stuck-at-1 conditions are modeled in HDL and detected by comparing the response of the circuit under test with stored reference data. The design is implemented and evaluated in Xilinx ISE on a Virtex-6 target. The synthesis report shows 512 slice registers, 12,142 slice LUTs, 348 fully used LUT-FF pairs, 24 bonded I/Os, two clock buffers, and one DSP48E1. The reported critical path delay is 0.511 ns, consisting of 0.232 ns logic delay and 0.279 ns routing delay, while the power report gives a total power of 1.065 W. Compared with the baseline values included in the source design report, the proposed HML-BIST uses fewer slice registers and LUT-FF pairs and substantially lower reported power. The results demonstrate that activity-aware pseudorandom testing can provide a practical low-overhead self-test mechanism for multiplier-oriented FPGA designs.*

Keywords: Built-in Self-Test, BCD Multiplier, HML-BIST, LFSR, Activity Factor, Space Comparator, Stuck-at Fault, FPGA, Xilinx ISE, Low-Power Testing.

I. Introduction

The continuing increase in VLSI integration density has made testability a first-order design concern. Modern integrated circuits combine processors, memories, arithmetic blocks, and interface logic on a single device, which increases the difficulty and cost of applying exhaustive external tests. Built-in self-test addresses this problem by incorporating test-pattern generation and response analysis within the device itself. In a typical BIST arrangement, a test pattern generator stimulates the circuit under test (CUT), and an output response analyzer determines whether the observed behavior matches the expected behavior[1]-[3].

Although pseudorandom testing is attractive because it requires relatively little on-chip hardware, unconstrained pattern transitions can increase switching activity during test. The resulting test power may exceed the level seen during normal operation.[5] For designs that are power- or thermal-

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constrained, excessive switching can reduce the reliability of at-speed testing and can increase the risk of false failures. The source design therefore introduces an activity-factor control mechanism around LFSR-based pattern generation to reduce unnecessary switching while retaining the compact implementation benefits of pseudorandom BIST.

The work considered here focuses on a Hybrid Memory Logic BIST (HML-BIST) organization used with a BCD multiplier test environment. The multiplier-related logic is treated as the CUT within a self-test structure that also contains RAM, LFSR-based pattern sources, multiplexers, reference storage, and a space comparator.[6]-[8]. The implementation is evaluated using Xilinx ISE. The central contributions of the design are:

(i) an LFSR-based pattern generation structure with explicit activity-factor control;
(ii) independent test-pattern support for write data, write address, and read address operations;
(iii) stuck-at fault modeling and comparator-based fault indication; and
(iv) FPGA synthesis evaluation in terms of area, delay, and power.

Because the supplied source report does not provide a numeric fault-coverage percentage or a detailed gate-level description of the BCD arithmetic core, this paper does not introduce unsupported fault-coverage or multiplier-internal claims. Instead, it concentrates on the HML-BIST architecture, its implementation flow, and the synthesis and simulation results reported by the source.[9].

II. Background and Related Work

Design-for-testability (DFT) techniques improve controllability and observability so that manufacturing and in-system faults can be detected with manageable test cost. BIST is one of the most widely used DFT strategies because the test stimulus and response-analysis hardware can be placed close to the CUT. For logic BIST, LFSRs are commonly used as pseudorandom pattern generators because an n-stage LFSR can produce a long deterministic sequence with small hardware overhead. For memory-oriented BIST, address generation, read/write sequencing, and comparison logic are additionally required.

Low-power BIST research has primarily targeted the switching activity generated by test patterns. Methods include low-transition LFSRs, bit-swapping techniques, scan-chain partitioning, reseeding, clock-gating, and correlation-aware pattern generation. The common objective is to reduce the number of unnecessary transitions without sacrificing the ability to excite and observe modeled faults. The HML-BIST approach follows the same design principle but applies activity control directly to the LFSR-driven write/read pattern paths in a memory-logic test arrangement.

The source material also discusses conventional and modified multiple-input signature registers (MISRs), March memory-test algorithms, and scan-based LBIST structures. These provide useful background, but the final proposed architecture is centered on LFSR pattern generation, RAM-based test operations, and a space comparator. Accordingly, the implementation described in this paper isolates those elements that are directly supported by the proposed-method and results chapters of the source.

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III. Proposed HML-BIST Architecture

3.1 System Organization:

Figure 1 presents a cleaned representation of the proposed architecture. Three LFSR paths provide pseudorandom values associated with write data, write address, and read address operations. Multiplexers select between functional inputs and BIST-generated inputs. The selected values are applied to the RAM/CUT test environment. A reference-data path supplies the expected values to a space comparator, which compares the observed response with the expected response and generates the final data-out or fault indication.

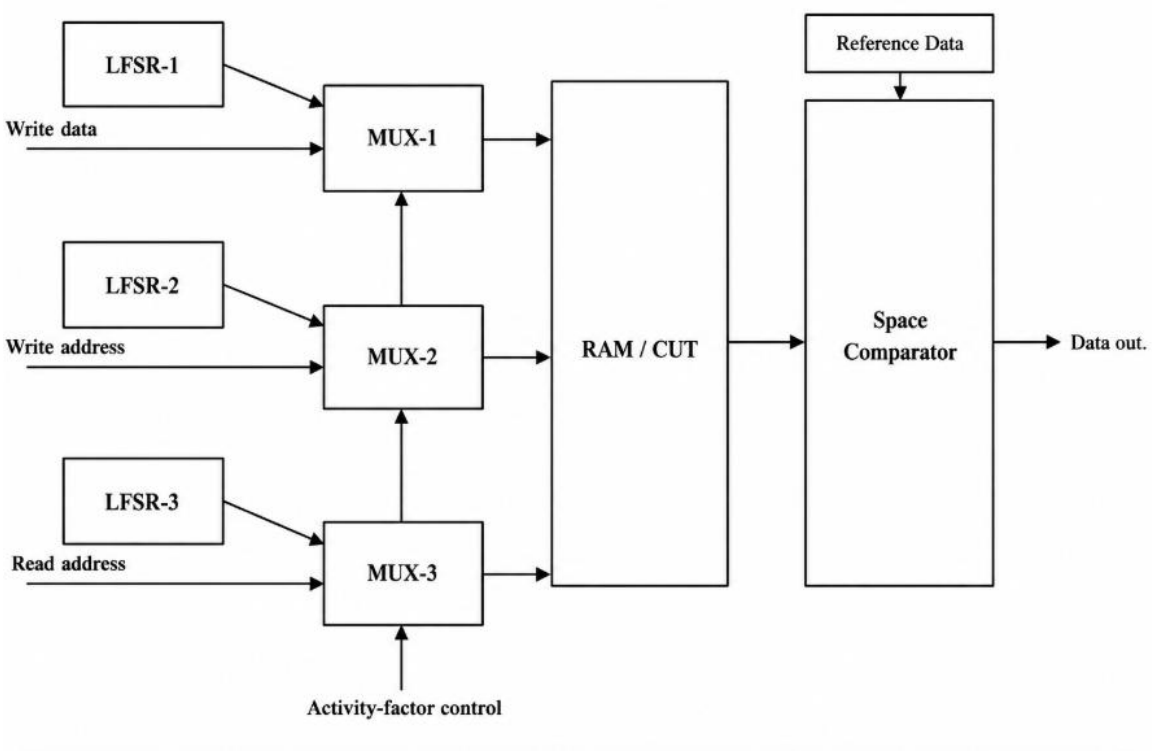

Figure 1: *Proposed HML-BIST organization used for the multiplier test environment (redrawn from the supplied design)*

3.2 Activity-Controlled LFSR Test-Pattern Generation:

An LFSR is formed from a chain of clocked storage elements and XOR feedback connections. Its compact structure makes it well suited to pseudorandom pattern generation. In the proposed design, LFSR outputs are not used only as unconstrained test vectors; the pattern paths are coupled with an activity-factor control input. The control can increase or decrease the allowed activity level during a BIST session, which provides a direct mechanism for reducing unnecessary pattern transitions.

The motivation can be expressed using the standard CMOS dynamic-power relation $P\_dyn \approx \alpha C\_L V\_DD^2 f$, where α is the switching-activity factor, C_L is the effective switched capacitance, V_DD is supply voltage, and f is operating frequency. Reducing α is therefore a direct way to reduce the dynamic component of test power when the other parameters are unchanged.

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The source implementation exposes the control through the signals af_red_inc and af_amount. A load signal transfers the selected activity amount, while af_red_inc changes whether the activity factor is increased or decreased. The up_down signal is used for count direction, and the program-counter/enable controls determine whether the test controller advances.

3.3 Space Comparator and Stuck-at Fault Detection:

The response-analysis function is implemented with a space comparator. During a test cycle, the value read from the RAM/CUT path is compared against stored reference data. A mismatch indicates that the observed response does not agree with the expected response. For an m-bit comparison word, the decision can be expressed as E = OR_i (y_i XOR r_i), where y is the observed response, r is the reference response, and E = 1 denotes a mismatch. This representation captures the comparator behavior without assuming a specific internal implementation.

The fault model used in the supplied implementation is the single stuck-at model. Stuck-at-0 and stuck-at-1 conditions are introduced in HDL so that selected internal or output values are forced to a constant logic level. The comparator output is then used to identify whether the test response departs from the reference data. The source report describes this mechanism as supporting fault detection and subsequent memory correction for the modeled scenarios.

3.4 BIST Execution Sequence:

1. Determine the number of CUT inputs and outputs required by the test configuration.
2. Generate the required set of test patterns from the configured pseudorandom generator.
3. Store or make available the expected response associated with each applied test condition.
4. Apply a test pattern to the CUT through the BIST-controlled input path.
5. Capture the CUT response and compare it with the corresponding reference value.
6. If no mismatch is detected, advance to the next test pattern.
7. Check whether the configured test sequence has completed.
8. If all patterns complete without a mismatch, assert the BIST-pass condition.
9. If a mismatch is observed, assert the BIST-fail indication and preserve the fault information for corrective handling.

IV. FPGA Implementation and Experimental Setup

The design was described in HDL and processed in Xilinx ISE. The source project flow includes project creation, source-file addition, behavioral simulation in ISim, RTL inspection, synthesis, timing analysis, and power estimation. The proposed implementation is reported for a Xilinx Virtex-6 device; the power-summary screenshot identifies an XC6VLX75T target in the FF484 package. The testbench stimulates the controller inputs clk, reset, enable, pc, af_red_inc, up_down, load, and af_amount, while bist_out indicates the pass/fail state.

The RTL schematic in Figure 2 shows the implemented controller hierarchy, including a pseudorandom pattern generator (PRPG), phase shifter, scan/test path, self-healing scan-cell block, CUT, test response analyzer, MISR-related response logic, and a space-comparator path. Although the internal

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schematic contains blocks inherited from the larger test-controller design, the results chapter evaluates the completed HML-BIST implementation as a single synthesized FPGA design.

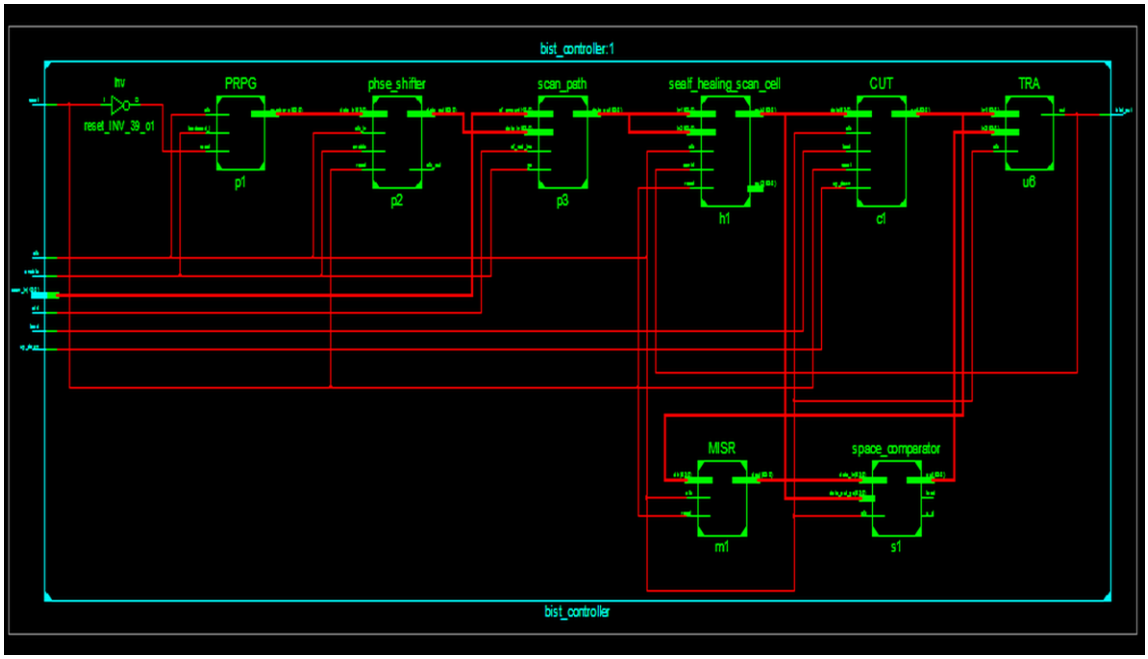

Figure 2: RTL schematic of the implemented BIST controller from Xilinx ISE

V. Results and Discussion

5.1 Resource utilization:

The device-utilization report is reproduced in Figure 3 and summarized in Table I. The proposed implementation uses 512 slice registers out of 35,200 available, 12,142 slice LUTs out of 17,600, 348 fully used LUT-FF pairs out of 12,306, 24 bonded I/O blocks out of 100, two BUFG/BUFGCTRL resources out of 32, and one DSP48E1 out of 80. The relatively low register and LUT-FF pair counts are consistent with the source claim that the controller overhead is reduced compared with the listed BIST baselines. The LUT count is substantially higher than the register count, which indicates that the implemented control and combinational test logic is LUT-dominant.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	512	35200	1%
Number of Slice LUTs	12142	17600	68%
Number of fully used LUT-FF pairs	348	12306	2%
Number of bonded IOBs	24	100	24%
Number of BUFG/BUFGCTRLs	2	32	6%
Number of DSP48E1s	1	80	1%

Figure 3: Xilinx ISE device-utilization summary for the proposed HML-BIST

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Table 1: FPGA resource utilization reported for the proposed HML-BIST

Resource	Used	Available	Reported utilization
Slice registers	512	35,200	1%
Slice LUTs	12,142	17,600	68%
Fully used LUT-FF pairs	348	12,306	2%
Bonded IOBs	24	100	24%
BUFG/BUFGCTRL	2	32	6%
DSP48E1	1	80	1%

5.2 Timing Performance:

The timing report in Figure 4 identifies a total data-path delay of 0.511 ns between the reported source and bist_out. Of this total, 0.232 ns (45.4%) is attributed to logic delay and 0.279 ns (54.6%) to routing delay. The slightly larger routing component shows that interconnect contributes more than half of the measured path delay, which is important when considering future placement-and-routing optimization.

```
Data Path: u6/out to bist_out
                              Gate     Net
  Cell:in->out      fanout   Delay    Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   FD:C->Q               1   0.232    0.279  u6/out (u6/out)
   OBUF:I->O                 0.000           bist_out_OBUF (bist_out)
  ----------------------------------------
  Total                      0.511ns (0.232ns logic, 0.279ns route)
                                     (45.4% logic, 54.6% route)
```

Figure 4: Timing summary: 0.511 ns total delay, comprising 0.232 ns logic and 0.279 ns routing.

5.3 Functional Simulation:

Figure 5 shows the ISim waveform used to verify controller operation. Reset, enable, program-counter, activity-factor increment/decrement, up/down direction, load, and activity amount are exercised while the clock runs continuously. The source description states that the active-high reset initializes the system, the enable/program-counter controls gate normal test progression, load captures af_amount, af_red_inc changes the activity factor, and up_down changes the counting direction. The bist_out signal provides the final BIST status, with the high state corresponding to pass and the low state corresponding to fail in the reported simulation.

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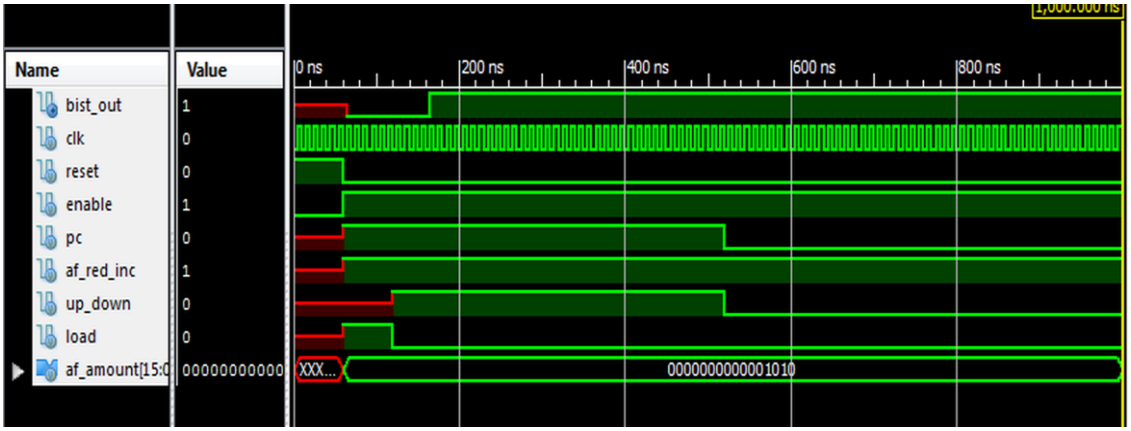
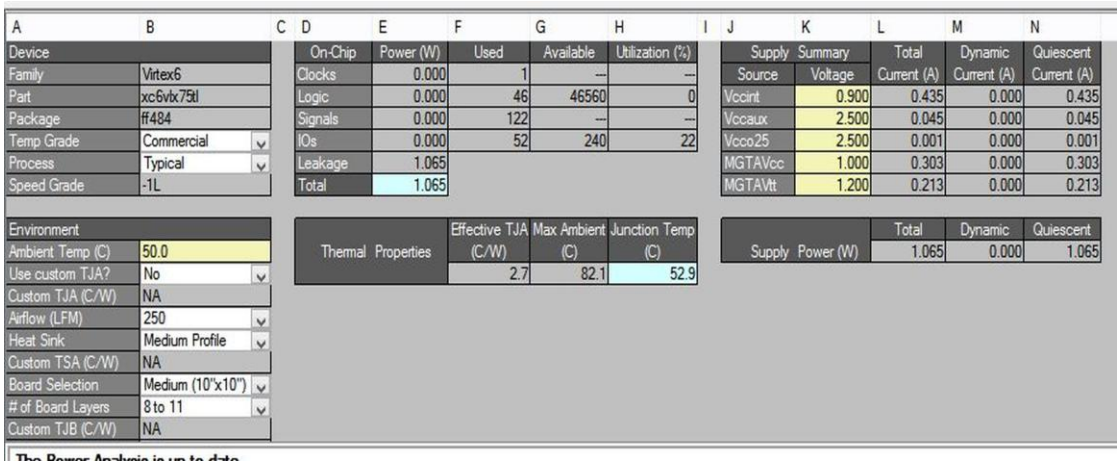


Figure 5: Behavioral simulation waveform of the proposed HML-BIST control signals

5.4 Power Analysis:

The Xilinx power report shown in Figure 6 gives a total estimated power of 1.065 W. The report is dominated by quiescent/leakage power for the selected Virtex-6 configuration; the screenshot lists 1.065 W leakage and a total of 1.065 W, with the dynamic entries shown as approximately zero for the analyzed condition. This result should therefore be interpreted as the power estimate associated with the supplied analysis setup rather than as a complete activity-annotated dynamic power characterization.



Device	
Family	Virtex6
Part	xc6vlx75tl
Package	ff484
Temp Grade	Commercial
Process	Typical
Speed Grade	-1L

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	--	--
Logic	0.000	46	46560	0
Signals	0.000	122	--	--
IOs	0.000	52	240	22
Leakage	1.065			
Total	1.065			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	0.900	0.435	0.000	0.435
Vccaux	2.500	0.045	0.000	0.045
Vcco25	2.500	0.001	0.000	0.001
MGTAVcc	1.000	0.303	0.000	0.303
MGTAVtt	1.200	0.213	0.000	0.213

Environment	
Ambient Temp (C)	50.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	8 to 11
Custom TJB (C/W)	NA

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	2.7	82.1	52.9

Supply Power (W)	Total	Dynamic	Quiescent
	1.065	0.000	1.065

Figure 6: Xilinx power summary for the proposed HML-BIST implementation

5.5 Comparison with the baselines reported in the source:

The source report provides comparative values for MBIST, PSRG-BIST, FT-BIST, and the proposed HML-BIST. Those values are reproduced in Table II. Because the source does not fully document whether all baseline implementations were synthesized under identical device, clock, activity, and power-analysis conditions, the comparison is treated as a reported baseline comparison rather than as an independently reproduced head-to-head experiment.

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Table 2: Performance comparison reproduced from the source report

Architecture	Slice registers	LUT-FF pairs	Power (W)
MBIST	784	826	32.482
PSRG-BIST	734	736	24.1939
FT-BIST	673	635	16.937
Proposed HML-BIST	512	348	1.065*

**The Xilinx power-summary screenshot and narrative report 1.065 W; the embedded comparison chart stores 1.1065 W. The synthesis-report value is used here*

Using the Table II values, the proposed design reports 34.7% fewer slice registers than MBIST, 30.2% fewer than PSRG-BIST, and 23.9% fewer than FT-BIST. The reductions in LUT-FF pairs are 57.9%, 52.7%, and 45.2%, respectively. The reported power is also markedly lower: 96.7% below MBIST, 95.6% below PSRG-BIST, and 93.7% below FT-BIST. These percentages describe only the numerical values contained in the supplied comparison and should not be interpreted as technology-normalized improvements unless the baseline implementation conditions are confirmed to be identical.

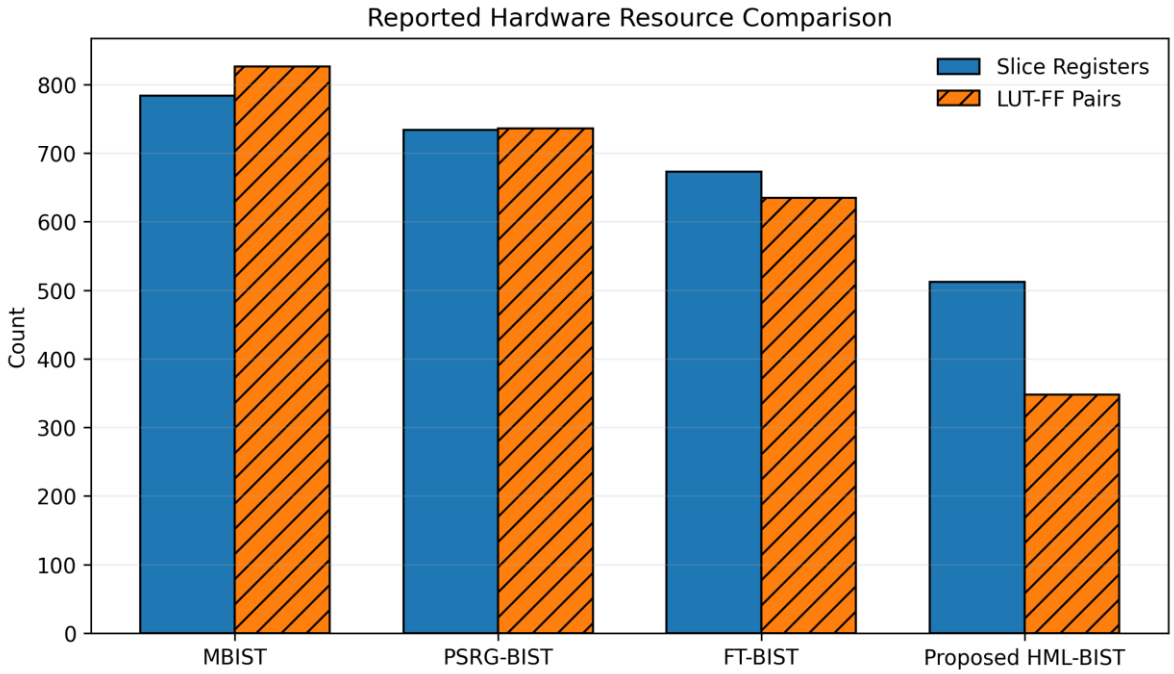

Figure 7: Comparison of reported slice-register and LUT-FF-pair counts

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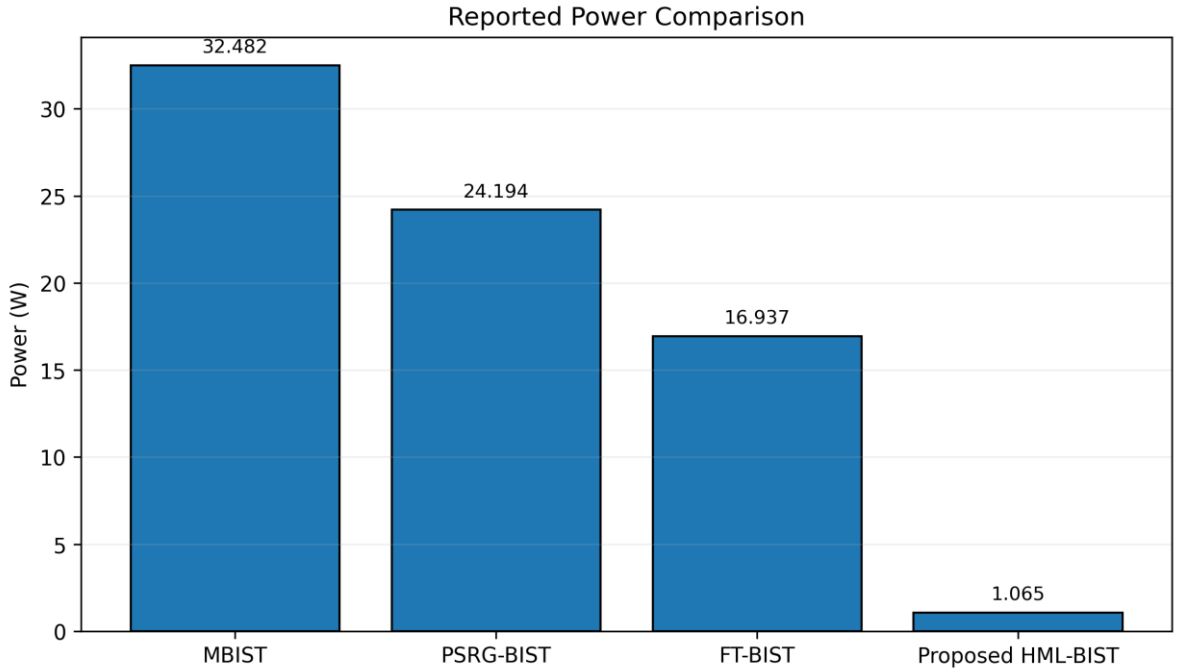

Figure 8: Comparison of reported power values. The proposed value uses the 1.065 W synthesis power summary

5.6 Discussion and Limitations:

The combined results support the intended design direction: a compact state/control structure, LFSR-driven test generation, and activity-factor regulation can be integrated into a practical FPGA self-test implementation. The 0.511 ns path delay indicates a short reported timing path, and the area report shows particularly low register and LUT-FF-pair utilization. The main quantitative limitation is that the source does not provide an explicit fault-coverage percentage, a list of injected fault sites, a test-pattern count, or baseline timing values under a common setup. Therefore, the present paper deliberately avoids claiming a specific fault-coverage number or a technology-normalized speedup.

A second limitation is that the supplied title identifies a BCD multiplier, whereas the results chapter emphasizes the HML-BIST controller and RAM/comparator infrastructure rather than the internal arithmetic realization of the BCD multiplication algorithm. A future publication should document the BCD multiplier datapath, decimal-correction logic, operand widths, fault-injection locations, and the relationship between arithmetic outputs and the reference-data mechanism. These additions would make the multiplier-specific contribution independently reproducible.

VI. Conclusion and Future Work

This paper has presented a power-efficient HML-BIST architecture for a BCD multiplier test environment based on LFSR-driven pattern generation, activity-factor control, RAM-based test operations, and a space comparator. The design models stuck-at-0 and stuck-at-1 conditions in HDL and uses the comparator response to indicate whether the observed behavior matches the stored

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reference behavior. Xilinx ISE implementation results report 512 slice registers, 12,142 slice LUTs, 348 fully used LUT-FF pairs, a total path delay of 0.511 ns, and an estimated power of 1.065 W. The baseline comparison supplied with the design also reports lower register, LUT-FF, and power values for HML-BIST than for MBIST, PSRG-BIST, and FT-BIST.

Future work should strengthen the evaluation by reporting deterministic fault-injection campaigns and numeric fault coverage, using activity-annotated power analysis, repeating all baseline implementations on the same FPGA and tool settings, and documenting the BCD multiplier datapath in detail. Additional extensions can include March-test integration for memory faults, optimized reseeding to reduce test length, adaptive activity-factor control based on measured switching, and formal verification of the BIST pass/fail controller.

References

[1] W. M. Abramovici, M. A. Breuer, and A. D. Friedman, Digital Systems Testing and Testable Design. New York, NY, USA: IEEE Press, 1990.

[2] M. Senthil Kumar and M. Javeed, “Design of NoC router with 3PE, double and triple error detection by using improved Hamming code,” ARPN Journal of Engineering and Applied Sciences, vol. 14, no. 16, pp. 2874–2880, Aug. 2019.

[3] T. Saraswathi, K. Ragini, and Ch. Ganapathy Reddy, “A review on power optimization of linear feedback shift register (LFSR) for low power built in self test (BIST),” in Proc. 3rd Int. Conf. Electronics Computer Technology (ICECT), vol. 6, pp. 172–176, 2011, doi: 10.1109/ICECTECH.2011.5942075.

[4] M. Javeed and M. Senthil Kumar, “Automatic brain tumour detection using new structure algorithm,” International Journal of Innovative Technology and Exploring Engineering (IJITEE), vol. 8, no. 11, pp. 3402–3405, Sep. 2019.

[5] P. K. John and P. Rony Antony, “Optimized BIST architecture for memory cores and logic circuits using CLFSR,” in Proc. Int. Conf. Intelligent Computing, Instrumentation and Control Technologies (ICICICT), pp. 1266–1270, 2017, doi: 10.1109/ICICICT1.2017.8342751.

[6] MD. Javeed and F. Jabeen, “FPGA implementation for the linking of cell tracks using new structure algorithm,” International Journal of Engineering and Advanced Technology (IJEAT), vol. 9, no. 1, pp. 6773–6778, Oct. 2019.

[7] B. Mishra, R. Jain, and R. Saraswat, “Low power BIST based multiplier design and simulation using FPGA,” in Proc. IEEE Students’ Conf. Electrical, Electronics and Computer Science (SCEECS), pp. 1–6, 2016, doi: 10.1109/SCEECS. 2016.7509284.

[8] MD. Javeed and C. F. Jabeen, “Linking of cell tracks using segmentation,” International Journal of Innovative Technology and Exploring Engineering (IJITEE), vol. 9, no. 1, pp. 3020–3026, Nov. 2019.

[9] B. Kaczmarek, G. Mrugalski, N. Mukherjee, A. Pogiel, J. Rajski, L. Rybak, and J. Tyszer, “LBIST for automotive ICs with enhanced test generation,” IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 41, no. 7, pp. 2290–2300, 2022, doi: 10.1109/TCAD.2021.3100741.

